DERWENT-ACC-NO: 2003-247214

DERWENT-WEEK: 200324

TITLE: Formation of wafer level package involves coating photo sensitive polymer on metal pad, forming trenches, filling material in trenches, grinding second surface of wafer, and reflow solder

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PATENT-ASSIGNEE: MOU E[MOUEI] , YANG W[YANGI]

PRIORITY-DATA: 2001US-0029764 (October 22, 2001) , 2001US-0846468 (April 30, 2001)

PATENT-FAMILY:

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APPLICATION-DATA:

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US20020160597A1	CIP of	2001US-0846468	April 30, 2001
US20020160597A1	N/A	2001US-0029764	October 22, 2001

INT-CL (IPC): H01L021/44

ABSTRACTED-PUB-NO: US20020160597A

BASIC-ABSTRACT:

NOVELTY - A wafer (2) level package is formed by coating a photo sensitive polymer (8) on a metal pad, forming trenches in between of

the packaging
entity, filling material in the trenches and covering
circuit distribution
diagrams, grinding a second surface of the wafer until the
filling material is
executing a solder screen printing step, and reflow the
solder to form a
conductive bump.

DETAILED DESCRIPTION - Method of forming wafer level
package for producing a
chip size packaging comprises:

(1) providing dies on the wafer (2), where the wafer has
I/O metal pads (4) on
a first surface;

(2) coating a photo sensitive polymer (8) on the first
surface;

(3) removing a portion of the photo sensitive layer to
expose the metal pad;

(4) coating a photoresist on a second surface of the wafer;

(5) forming a conductive seeding layer (14) on the top of
the first conductive
layer and the photosensitive polymer;

(6) patterning a photoresist on top of the seeding layer to
define a circuit
pattern;

(7) forming a second conductive layer on the photoresist
pattern to serve as
the circuit distribution diagram;

(8) removing the photoresist pattern and the seeding layer
beneath;

(9) forming trenches in between of the packaging entity;

(10) filling material in the trenches and covering the
circuit distribution
diagrams;

(11) grinding the second surface until filling material is
exposed;

(12) executing an opening step to expose a portion of circuit distribution
diagram to define a reserved area for a conductive bump;

(13) executing a solder (24) screen printing step to form a layer of solder on
the reserved area; and

(14) reflow the solder to form a conductive bump.

USE - For the formation of a wafer level package (claimed) for producing a chip
size packaging.

ADVANTAGE - The invention is simple and compact.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional diagram of the
wafer after cutting the level package.

Wafer 2

Metal pads 4

Photo sensitive polymer 8

Conductive seeding layer 14

Solder layer 24

CHOSEN-DRAWING: Dwg.13/13

TITLE-TERMS: FORMATION WAFER LEVEL PACKAGE COATING PHOTO SENSITIVE POLYMER
METAL PAD FORMING TRENCH FILL MATERIAL TRENCH GRIND SECOND SURFACE
WAFER REFLOW SOLDER

DERWENT-CLASS: A89 G06 L03 U11

CPI-CODES: A12-E07C; A12-L02B2; G06-D06; G06-E; G06-E04; G06-F03C; G06-G17;
G06-G18; L04-C17;

EPI-CODES: U11-C05G2B; U11-C08A3; U11-D01A8; U11-D03B1;

ENHANCED-POLYMER-INDEXING:

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Polymer Index [1.2]
018 ; P0464*R D01 D22 D42 F47
Polymer Index [1.3]
018 ; ND01 ; Q9999 Q8673*R Q8606 ; ND07 ; N9999 N7147 N7034 N7023
; Q9999 Q7114*R ; K9483*R ; Q9999 Q8684 Q8673 Q8606 ; N9999 N7283
; B9999 B5425 B5414 B5403 B5276 ; K9552 K9483 ; Q9999 Q7476 Q7330

SECONDARY-ACC-NO:
CPI Secondary Accession Numbers: C2003-063585
Non-CPI Secondary Accession Numbers: N2003-196445

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(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2002/0160597 A1

Yang et al. (43) Pub. Date: Oct. 31, 2002

(54) WAFER LEVEL PACKAGE AND THE PROCESS OF THE SAME

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(22) Filed: Oct. 22, 2001

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Publication Classification

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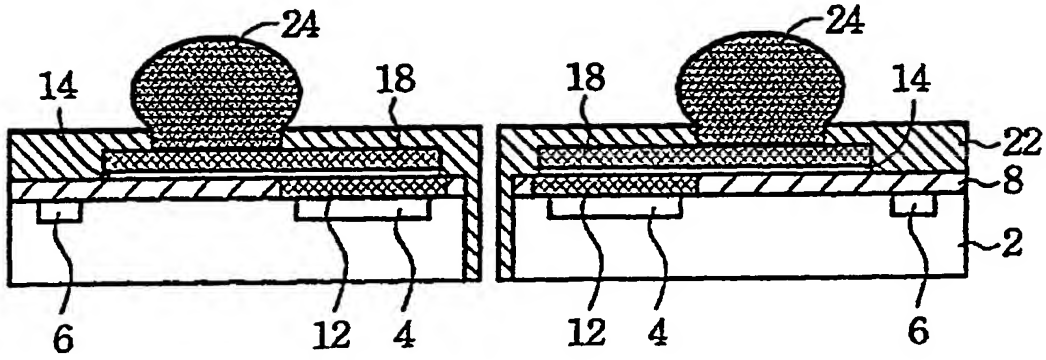
(52) U.S. Cl. 438/613; 438/612; 438/614; 257/685

(57) ABSTRACT

The present invention comprises a plurality of dies formed on the wafer and an I/O metal pad formed on the first surface of the wafer. Then, photo PI is coated on the first surface, then a portion of the PI is removed by laser. Next step, a first photoresist is coated on the second surface of the wafer and the photoresist includes positive photoresist. A first conductive layer is formed in the hole of the photo PI and covers a metal pad. Subsequently, a seeding layer with copper is formed on the top of the first conductive layer and the photo sensitive polymer layer. Then, a second photoresist is formed on the seeding layer to define the circuit pattern diagram. Then, a second conductive layer is formed. Next step is to remove the second and the first photoresist covered by the second photoresist, thereby forming trenches therein. Then, the filling material is filled into the trench and covers the circuit pattern diagram. A grinding process is performed to grind the second surface of the wafer to expose the filling material. Next step is to expose a portion of the circuit pattern to define an area formed by the conductive convex block. A solder screen printing step is used to form a solder on the defined area. The solder is re-flowed to form conductive bump.



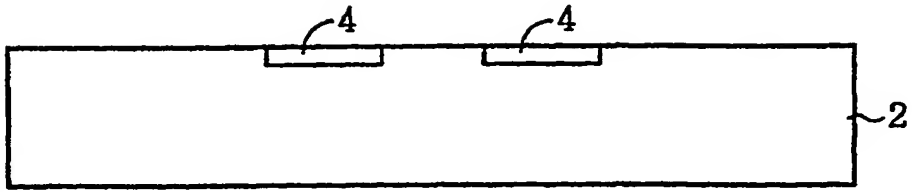


FIG. 1

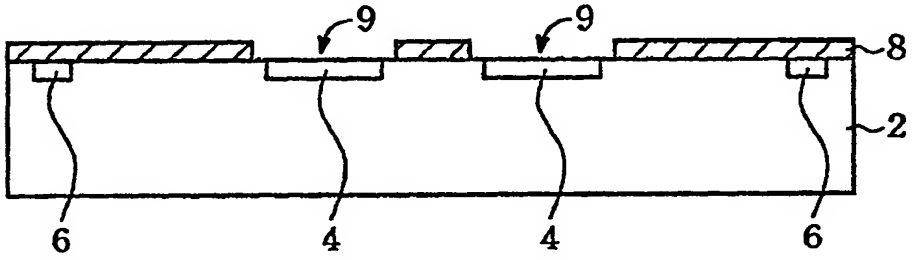


FIG. 2

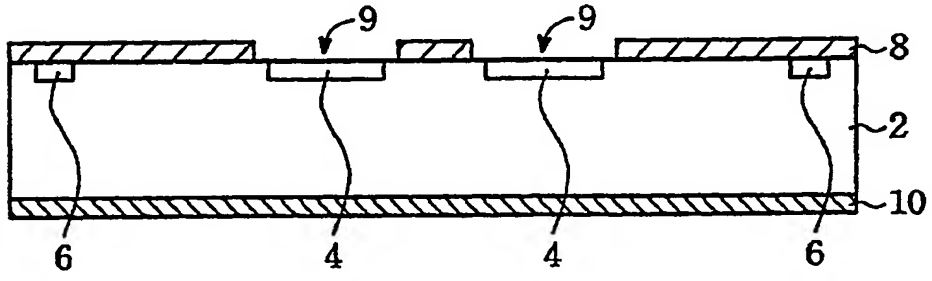


FIG. 3

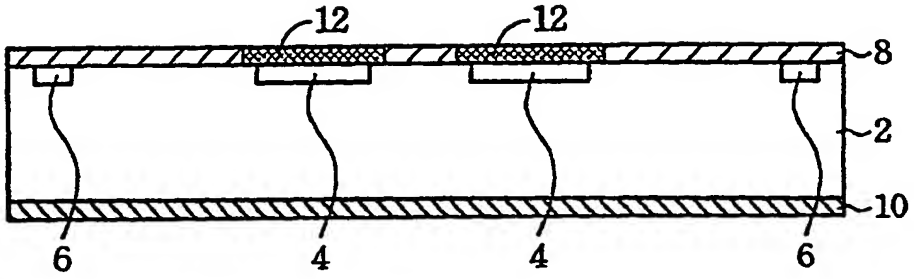


FIG. 4

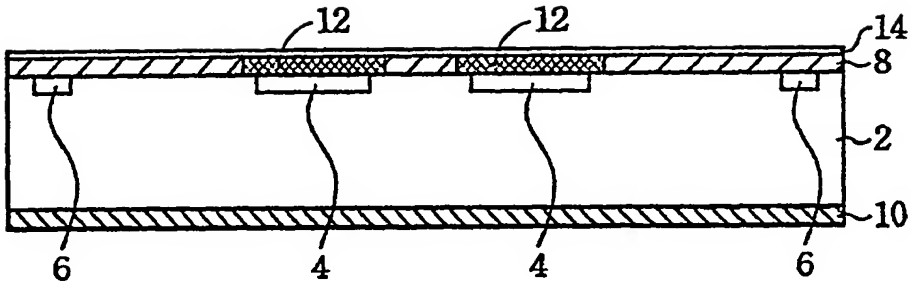


FIG. 5

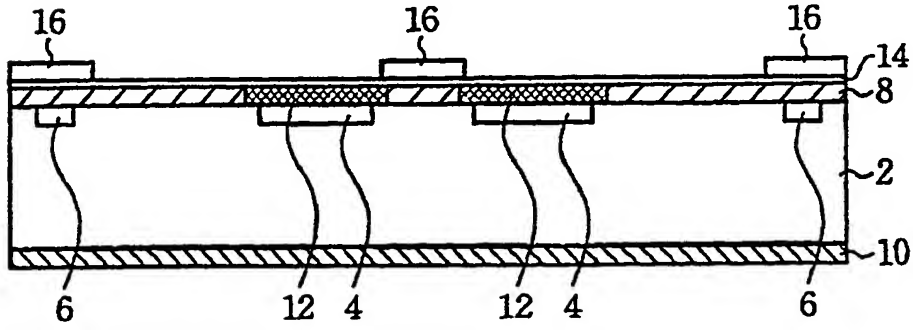


FIG. 6

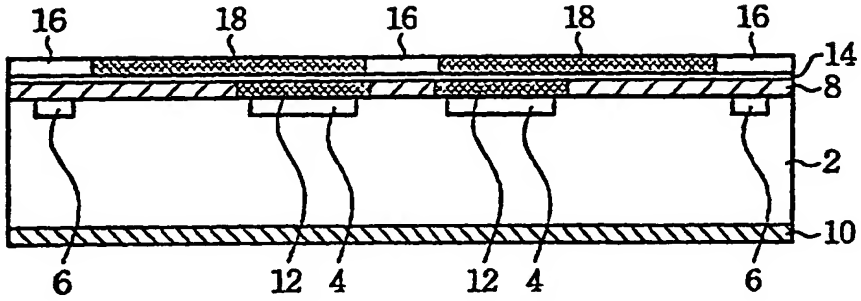


FIG. 7

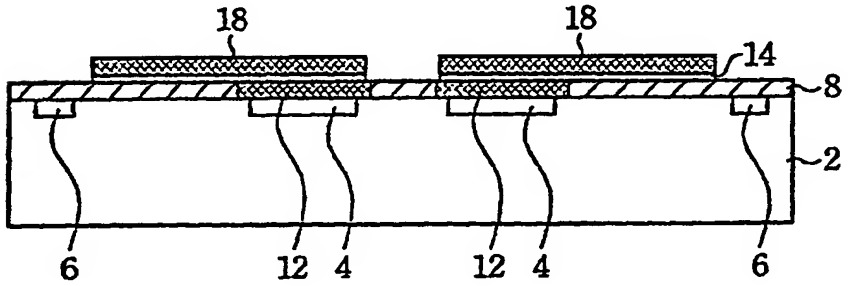


FIG. 8

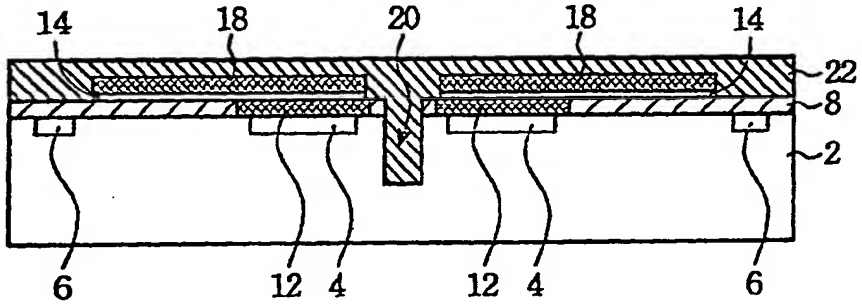


FIG. 9

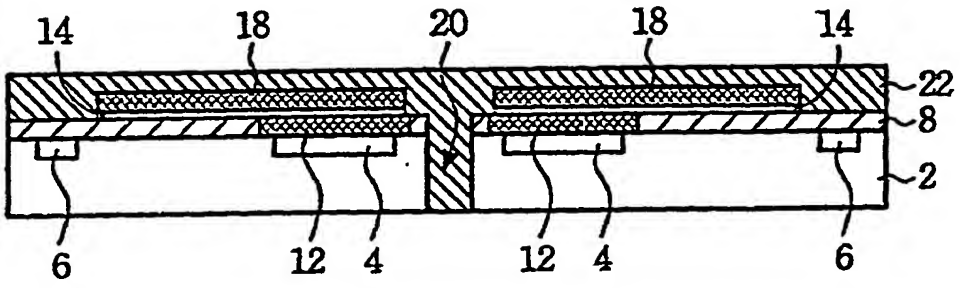


FIG. 10

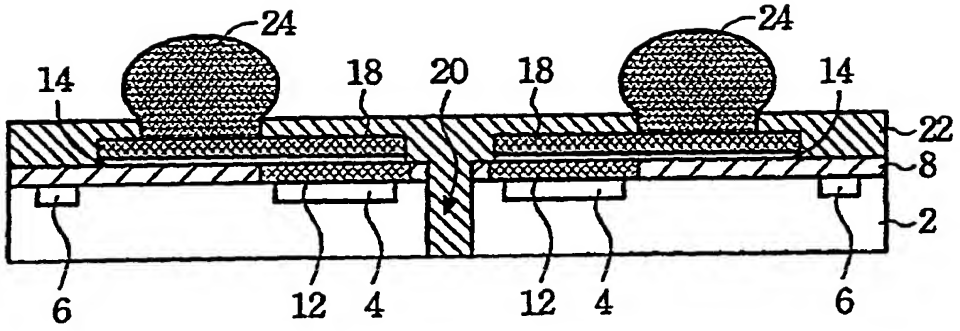


FIG. 11

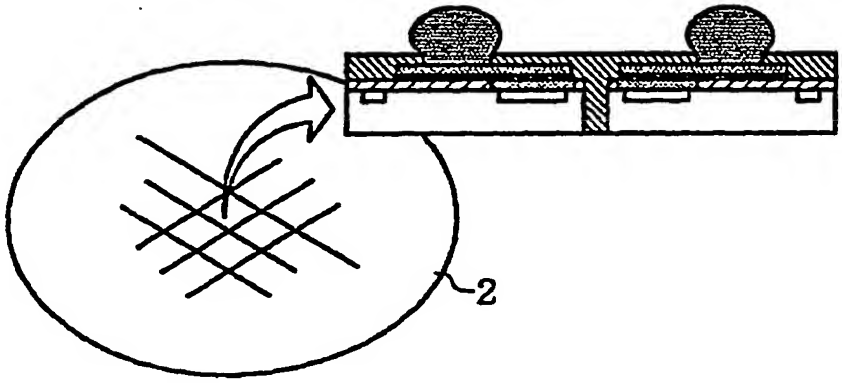


FIG. 12

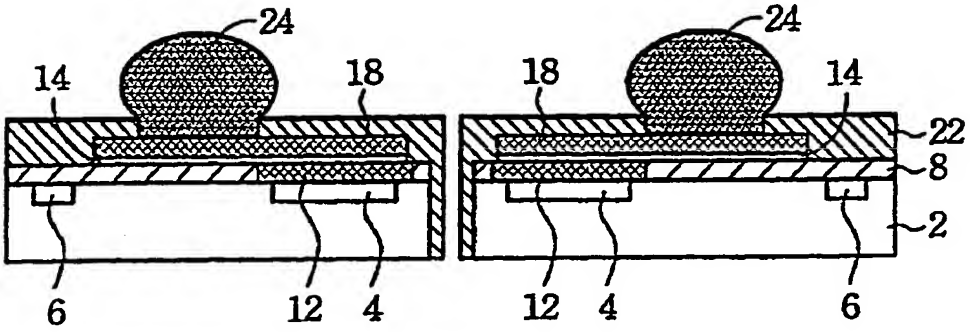


FIG. 13

WAFER LEVEL PACKAGE AND THE PROCESS OF THE SAME

FIELD OF THE INVENTION

[0001] This present invention relates to a semiconductor package, and more specifically, to a wafer level packaging technology and the method for forming the wafer level package.

BACKGROUND

[0002] In recent progress of integrated circuit device, since the chips are manufactured by a trend of high density and it also has a trend to make semiconductor devices have smaller size in order to contain more IC in the devices. IC designers are attempted to scale down the size of devices and increase chip integration in a much smaller space. Typically, the semiconductor devices need a protection to prevent the penetration of moisture or the damage caused by accidentally damage. Owing to this, the device structure needs to be packaged by some appropriate technology. In this technology, the semiconductor dies or chips are usually packaged in a plastic or ceramic package. The package of the chips must have the function to protect the chips from being damaged and to release the heat generated by the chips while they are under operation.

[0003] The previous packaging technology was mainly on the concept of the lead frame, using the lead leg as the I/O signal exchange channel. But now, under the highly integrated requirement of the I/O signal exchange, the traditional lead frame packaging can't totally meet the demand of this requirement. Under this consideration, the packaging needs to be smaller in volume in order to meet the highly integrated requirement. Highly integrated I/O packaging concept also brings the development and a breakthrough in the package technology. A method named as ball grid array (BGA) technology is a popular used method in recent year. Integrated circuit (IC) manufacture companies tend to adapt ball grid array (BGA) technology due to the lead leg used by BGA is a ball shaped leg instead of the slender leg used by the traditional lead frame technology. Another advantages of BGA also includes that the pitches (distance between balls) are smaller and is not easily deformed because of their ball shaped legs. The smaller distances between balls reveals that the signal transportation would also become quicker than the traditional lead frame technology The U.S. Pat. No. 5,629,835, proposed by Mahulikar, et. all, which entitled "METAL BALL GRID ARRAY PACKAGE WITH IMPROVED THERMAL CONDUCTIVITY" states a ball grid array packaging method. Another U.S. Pat. No. 5,239,198 discloses a packaging form, which consists a substrate using FR4 material to form the screen printing package.

[0004] The various integrated circuit packaging have been developed in recent years, however no matter what kind it is. Most of them adapt the following procedure in dividing the wafer: First, cutting the wafer into individual chips then proceed the packaging and testing step. However, in U.S. Pat. No. 5,323,051 "SEMICONDUCTOR WAFER LEVEL PACKAGING", it reveals a packaging step. The packaging step is conducted before cutting the wafers. it uses glass as adhesive material to seal the device in a hole. A covered hole is allowed to be the electric channel. The wafer level packaging is another manufacture trend for semiconductor package. One of the previous inventions is to form a plurality of dies on a surface of a semiconductor wafer. A glass is attached on the surface of the wafer having dies formed thereon. Then the other surface of the wafer (the surface without dies) is grinded to reduce the thickness of the wafer. This method is called back grinding. Then, the wafer is etched to separate from IC and expose a portion of the adhesive material. Another glass is attached to the wafer surface with dies by adhesive material. The next step is to form a thin film on the first glass, then etching the first glass and a portion of the adhesive material. This step is called the notch process. Thus forming a trench in the glass and adhesive material. In the next sep, Tin ball will be formed on the thin film in the subsequent process. The thin film made by solder will be patterned onto the surface of the first glass and the surface along the trench to provide an electric connection channel. Solder mask is then formed on the surface of the solder thin film surface and the surface of glass to expose the surface for which it is associated with the thin film. Tin ball is formed on the exposed solder thin film by traditional method. In the next step, the cutting procedure is conducted by etching the adhesive material in the trench to cut through the glass in order to separate the dies. The method mentioned above is complicate, it need the notch process and cutting the second glass to separate the dies. Besides, the cutting place would become a trench cliff, which is sharp for solder to attach on the cutting place and finally reduce the quality of the device in package process.

[0005] According to the reasons mentioned above, there is a need to provide a more simple and compact method to the wafer level packaging.

SUMMARY

[0006] It is an objective of the invention to provide a chip size packaging.

[0007] It is another objective of the invention to provide a wafer level package method.

[0008] It is yet another objective of the invention to provide a wafer level package method suit for the wafer level packaging test.

[0009] The wafer level package comprising: a plurality of dies formed on the wafer, an I/O metal pad formed on the first surface of the wafer.

[0010] Then, coating a photo sensitive polymer, for example, photo PI film on the first surface, then a portion of the film is removed by laser.

[0011] In the next step, coating a first photoresist on the second surface of the wafer, said first photoresist comprising positive photoresist.

[0012] Forming a first conductive layer in the hole (opening) of the photo PI film and then cover a metal pad, the first conductive layer comprising alloy with the composition of Zn/Ni/Cu.

[0013] In the next step, forming a seeding layer with copper on the top of the first conductive layer and the photo sensitive polymer layer. Then, forming a second photoresist on the seeding layer to define the circuit pattern diagram. Then, forming a second conductive layer to the circuit pattern diagram located on the defined are of the second photoresist. The second conductive layer comprises copper.

[0014] Removing the second and the first photoresist and the seeding layer covered by the second photoresist, thus forming trenches between each of the packaging entity.

[0015] Then, the filling material was filled into the trench and covers the circuit pattern diagram. The filling material comprises EPOXY.

[0016] Then, executing the grinding process to grind the second surface of the wafer to expose the filling material. Next, executing an opening step to expose a portion of the circuit pattern diagram to define an area formed by the conductive convex block.

[0017] Executing a solder screen printing step to form a solder paste area, then reflowing this area to form a conductive convex block.

BRIEF DESCRIPTION OF THE DRAWING

[0018] The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

[0019] **FIG. 1** indicates the cross-sectional diagram of a wafer with metal pad formed thereon.

[0020] **FIG. 2** indicates the cross-sectional diagram of a wafer with an opening opened thereon.

[0021] **FIG. 3** indicates the cross-sectional diagram of a wafer with a positive photoresist formed on the back-side of the wafer.

[0022] **FIG. 4** indicates the cross-sectional diagram of a wafer with a electroplating pad wetting layer formed thereon.

[0023] **FIG. 5** indicates the cross-sectional diagram of a wafer with a non-electroplating copper seeding layer formed thereon.

[0024] **FIG. 6** indicates the cross-sectional diagram of a wafer with coating photoresist diagram thereon to define the circuit diagram.

[0025] **FIG. 7** indicates the cross-sectional diagram of a wafer with electroplating to form the copper layer.

[0026] **FIG. 8** indicates the cross-sectional diagram of a wafer with the situation of photoresist removed.

[0027] **FIG. 9** indicates the cross-sectional diagram of a wafer with trench and filling material filled formed therein.

[0028] **FIG. 10** indicates the cross-sectional diagram of a wafer with back-side grinding surface.

[0029] **FIG. 11** indicates the cross-sectional diagram of a wafer with Tin ball formed therein.

[0030] **FIG. 12** indicates the cross-sectional diagram of a wafer after the wafer level package testing.

[0031] **FIG. 13**. indicates the cross-sectional diagram of a wafer after cutting (dividing) of the wafer level package.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0032] This invention discloses a wafer level package and a method for manufacturing the wafer level package. The detail procedure is shown below: First referring to **FIG. 1** and **FIG. 2**, a surface (the first surface) of a wafer **2** has a metal pad for input and output signal (I/O pad) and a window **6** is also formed on the surface of the wafer for laser repair. Then, a photo sensitive polymer **8** is formed on the first surface of the wafer **2**. The preferred material for photo sensitive polymer **8** could be photo PI or EPOXY. A curing process by ultra violet radiation or heating process is conducted to enhance the structure of EPOXY. Then, forming a plurality of openings **9** in the insulator layer **8**, each opening area is opened associated with the metal pad **4**. These metal pads **4** are thus exposed with no coverage. It should be noticed that the photo PI or EPOXY are transparent material respect to laser, so the alignment mark on the scribble line will not be covered by the insulator layer **8**. In other words, the label is visible to the alignment tools and can be easily seen in the next operation.

[0033] Another way of forming an opening **9** in order to expose the metal pad **4** can also be conducted as follows: Using a mask with some certain pattern to transfer the pattern onto the photoresist, and after the etching process to remove the photo PI or EPOXY, this can also done to form the opening **9**.

[0034] Referring to **FIG. 3**, a photoresist **10** is coated on the second surface of the wafer **2**, and a wetting layer **12** is filled into to the opening **9**, and the material for wetting layer **12** can be metal or alloy such as Tin/Ni/Cu. Typically, the wetting layer **12** can be formed by electrical plating.

[0035] Next referring to **FIG. 5**, a copper seeding layer **14** could be used by electroless Cu plating method to implant the copper seeding layer **14** on the surface of the film **8** and the wetting layer **12**. Next, photoresist pattern **16** is coated on the copper seeding layer **14** to define metal wire pattern. In **FIG. 6**, using the photoresist pattern **16** as a barrier, the metal (copper) wire **18** is formed on the portion of the area which is an area not to be covered by the photoresist pattern **16**. The formation of the metal wire can be conducted using plating method or other method to form the pattern on the surface of the wafer **2**, as shown in **FIG. 7**. Next, removing the photoresist diagram **16** and the copper seeding layer **14**. During the removing step, although a very thin layer of copper layer **18** may be removed a little bit yet it would do little harm to the whole structure. In this way, the I/O metal pad **4** can be directed through thin film **12** to form an electric connection with the metal layer **18**. This process is called re-distribution.

[0036] Referring to **FIG. 9**, etching the surface of the wafer **2** thus forming a trench **20** which can be used in the further manufacture step. A filling material **22** is filled in the trench **20** to cover the metal wire **18** for insulation and adhesion for packaging entity. The filling material can be EPOXY coated by vacuum coating process. The vacuum coating process can prevent the occurrence of bubble formed therein. EPOXY filling material is filled in every packaging entity. In the next step, a curing process such as ultra violet radiation or heating process is conducted to enhance the EPOXY structure. A back-side wafer grinding process is conducted in the next step to grind the second surface (the side without circuit lie above) till the bottom of the trench **20** in order to expose the filling material **22**, as shown in **FIG. 10**.

[0037] Referring to **FIG. 11**, the next step is to define a bump area of solder ball. A portion area of the insulated

filling material **22** will be removed and to expose the wire pattern **18**. The exposed area of the wire diagram **18** is aimed to be the side location of the bump. The screen printing method is utilized to coat a layer of solder on the area and to reflow it by thermal process and turning a paste layer of solder into solder ball **24**. The solder ball **24** is thus attached to the wafer. The formation of solder ball **24** can be conducted by the well known BGA technology and distributed as an array pattern along the side of a chip. An electric channel is thus constructed by the connection of Tin ball **24** to metal wire diagram **18**. **FIG. 12** is the diagram showing the wafer level package testing procedure. The wafer **2** is sent to the wafer level testing device for final testing. After the final testing, the wafer is proceeding with a cutting (dividing) process to separate the chips. The cutting process is mainly cut along the trench of the filling EPOXY, thus producing a chip size package (CSP). This invention is simpler than the previous prior art and the advantages of the invention are the back side photoresist and the trench of the filling material can be easily tested before cutting process is conducted. And after the cutting process, it is easily cut along the trench to separate each chip on the wafer, as shown in **FIG. 13**.

[0038] The wafer level package of this invention is shown in **FIG. 11**, which possesses a plurality of chips on the wafer **2**. A trench **20** formed therein to run through the wafer. Filling material **22** is filled in the trench. Metal pad **4** is formed on the surface of the wafer **2**. Photo sensitive polymer **8**, such as photo PI or EPOXY is formed on the wafer **2** surface and exposed the metal pad **4**, the first conductive layer **12** lies within the insulated material **8**, the electric channel **18** lies above the surface of the insulator **22** and the first conductive layer **12**. A protection layer is covered on the top of the electric channel, insulated material and it also expose a portion of the electric channel and the conductive bump **24**, which is on the top of the exposed metal wire **18**.

[0039] As will be understood by persons skilled in the art, the foregoing preferred embodiment of the present invention is illustrative of the present invention rather than limiting the present invention. Having described the invention in connection with a preferred embodiment, modification will now suggest itself to those skilled in the art. Thus, the invention is not to be limited to this embodiment, but rather the invention is intended to cover various modifications and similar arrangements included within the spirit and scope of the appended claims, the scope of which should be accorded the broadest interpretation so as to encompass all such modification and similar structure.

[0040] While the preferred embodiment of the invention has been illustrated and described, it will be appreciated that various changes can be made therein without departing from the spirit and scope of the invention.

1. A method of forming wafer level package for producing a chip size packaging,

said method comprising:

providing a plurality of dies on the wafer, wherein said wafer has I/O metal pads on a first surface of said wafer;

coating a photo sensitive polymer on said first surface;

removing a portion area of said photo sensitive polymer to expose said metal pad;

coating a photoresist on a second surface of said wafer;

forming a first conductive layer in said photo sensitive polymer and covering said metal pad;

forming a conductive seeding layer on the top of said first conductive layer and said photo sensitive polymer;

patterning a photoresist on the top of said seeding layer to define circuit pattern;

forming a second conductive layer on said defined photoresist pattern to serve as the circuit distribution diagram;

removing said photoresist pattern, and removing the seeding layer covered by said photoresist pattern;

forming trenches in between of the packaging entity;

filling material in said trenches and covering said circuit distribution diagrams;

grinding said second surface of said wafer until said filling material is exposed;

executing an opening step to expose a portion of said circuit distribution diagram to define a reserved area for a conductive bump;

executing a solder screen printing step to form a layer of solder on said reserved area; and

reflow said solder to form a conductive bump.

2. The method according to claim 1, wherein after executing said reflowing process, further comprising testing said wafers.

3. The method according to claim 2, wherein after executing said testing, further comprising a cutting process along said trenches.

4. The method according to claim 1, wherein said photo sensitive polymer comprises photo PI.

5. The method according to claim 1, wherein said photo sensitive polymer comprises EPOXY.

6. The method according to claim 1, wherein said opening of said metal pad is formed by laser.

7. The method according to claim 1, wherein said first conductive layer comprises alloy with the composition of Zn/Ni/Cu.

8. The method according to claim 1, wherein the formation of said seeding layer is formed by using electroless copper plating.

9. The method according to claim 1, wherein said second conductive layer comprises copper.

10. The method according to claim 9, wherein said copper is formed by electroplating.

11. The method according to claim 1, wherein said filling material comprises EPOXY.

12. The method according to claim 1, further comprising a step to solidify said EPOXY.

13. A wafer level package comprising:

a plurality of chips on a wafer, said wafer has trench formed in said wafer and run through said wafer;

material filled in said trenches;

metal pad formed on the surface of said wafer;

photo sensitive polymer material formed on the surface of said wafer and expose said metal pad;

a first conductive layer formed within said photo sensitive polymer material;

circuit diagram patterning formed on the top of said photo sensitive polymer material and said first conductive layer;

a protection layer covered on said circuit diagram, said photo sensitive polymer material and a portion of said circuit diagram exposed; and

a conductive bump formed on said exposed circuit diagram.

14. The wafer level package according to claim 13, wherein said photo sensitive polymer comprises EPOXY.

15. The wafer level package according to claim 13, wherein said photo sensitive polymer comprises photo PI.

16. The wafer level package according to claim 13, wherein said filling material comprises EPOXY.

17. The wafer level package according to claim 13, wherein said protection layer comprises EPOXY.

18. The wafer level package according to claim 13, wherein said conductive pattern diagram comprises copper.

19. The wafer level package according to claim 13, wherein said conductive bump comprises solder.

* * * * *